SynQor

Advancing The Power Curve

Current Sharing and other Full-Feature Applications

Application Note 01-04-1 Rev. 01 - 5/10/01

Summary:

This application note provides detail on features available on SynQor's full-feature half-brick dc/dc converters. The central feature discussed in detail is the active current sharing. Other features discussed in this paper include Start Synchronization, External Clock Synchronization and the OR'ing FET drive function. Proper application of all full feature units, as well as circuit diagrams and schematics are included.

SynQor's *Power*Qor Full Feature Tera, Giga, Mega and Kilo DC-DC Converters

The parallel operation of multiple dc/dc converters in a power supply system is frequently desirable and advantageous. Paralleling converters increases the total power available while also improving the system reliability. Higher reliability is achieved from N+1 redundancy and the reduced stresses that result when modules are operated significantly below their rated limits. SynQor now offers the *Power*Qor family of Tera, Giga, Mega and Kilo half-brick dc/dc converters, which are available in a full-feature option that allows for current-sharing applications. This application note provides information to facilitate the successful implementation of SynQor's full feature modules in paralleled applications.

Figure 1 shows a *Power*Qor half-brick Tera, Giga, Mega or Kilo full-feature DC/DC converter. Refer to the technical data sheet for a more detailed description of the pins. Note that all the pins on the primary side, or left hand side of the module in the diagram, are referenced to the primary side ground, *Vin(-)*, and all the pins on the secondary side, or right hand side in the diagram, are referenced to the secondary side ground.

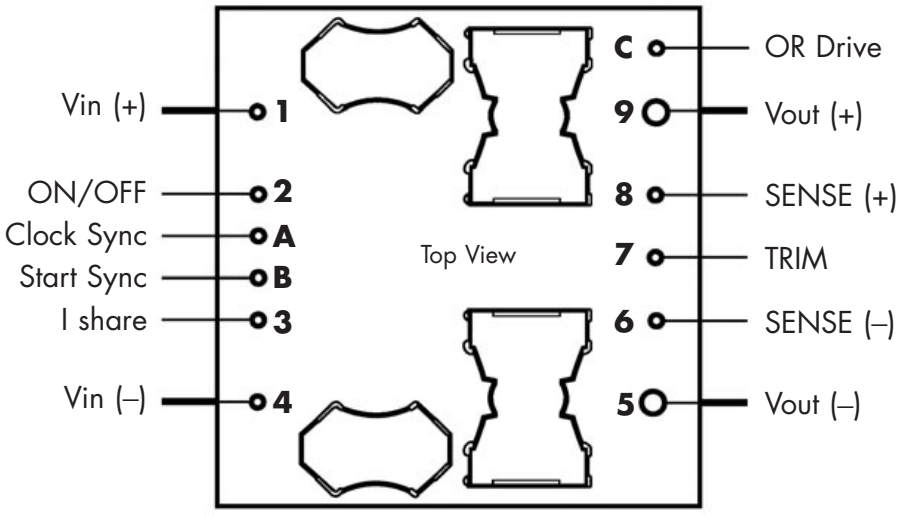

Figure 1: *Power*Qor Full-Feature Half Brick Converter

Master-Slave Current Sharing

When converters are paralleled passively, most of the load current is supplied by the unit with the highest output voltage. This current imbalance always happens because component tolerances ensure that the nominally equal output voltages of different units are always slightly different. Passively paralleled converters can be forced to share load current reasonably well, but only by sacrificing the output voltage regulation, which is an undesirable side effect. For this reason, all *Power*Qor full feature converters are paralleled actively using the master-slave method to simultaneously achieve tight current sharing and tight output voltage regulation that is comparable to that of a stand-alone unit.

Master-slave operation is achieved in *Power*Qor converters by connecting together the *Ishare* pins of the paralleled units to allow them to share load current information. A current feedback loop within each converter uses the information from the *Ishare* pin to control how much of the total load current it supplies. The unit with the highest output voltage, which in the absence of a current feedback loop would supply most of the current, assumes the role of a master, and the other units become slaves. Each of the slave units compares its output current to that of the master and tries to match it by adjusting its output voltage upward by the requisite amount. The master's current adjusts downward by the amount that the slaves' currents rise. The voltage at the common connection point of the *Ishare* pins is proportional to the average output current of one unit.

With master-slave current sharing the output voltage of the system is equal to the stand-alone voltage of the master unit, and the master's output current always remains slightly higher than that of any slave. When properly designed, this method is capable of forcing the output currents of the paralleled converters to track very closely.

All *Power*Qor full-feature modules, regardless of output voltage, typically share to better than 2% of the combined full load current. For example, the current imbalance between two paralleled 48Vin to 3.3Vout Tera converters is typically less than 2A at the combined full load current of 100A. Similarly, the imbalance between two 48Vin to 5.0Vout Kilo converters is typically less than 800mA at the combined full load current of 40A.

The current imbalance between the master and the slaves is proportional to the number of slaves. If, in a system with two converters, the master's output current is typically ΔI_O amperes greater than the slaves' output current, then in a system with a master and (N-1) slaves, each slave's average output current will typically be (N-1) • ΔI_O amperes lower than the master's output current. As an example, if three 48Vin to 3.3Vout Tera units are paralleled, and the master supplies 40A, then each slave will typically supply 36A. In converter families with large ΔI_O, the current imbalance (N-1) • ΔI_O can become large enough, even for small N, for the master to carry a disproportionate part of the load current. In *Power*Qor converters, ΔI_O is so small that the current imbalance remains reasonably small even for fairly large N.

The current imbalance between master and slaves is essentially load-independent down to very light loads of about 5%.

Note that if a non-redundant paralleled system's master is switched off, or fails without overloading the shared output voltage bus, then the converter with the next highest output voltage automatically assumes the master function and operation continues uninterrupted. A redundant system is even more tolerant to some of the converters failing.

Paralleling *Power*Qor Converters

*Power*Qor full feature dc/dc converters are paralleled as shown in Figure 2 below. The following pins on different converters must be tied together:

- Like input pins *Vin(-)* and *Vin(+)*. In most cases an input filter will be used between the input voltage source and the converters. The input pins of the converters, particularly the *Vin(-) pins*, must be connected together directly on the converters side of the filter, as shown in Figure 2. No component should be interposed between the *Vin(-)* pins of different units. The input filter should be situated exactly as shown in Figure 2, with the input source on the filter's input side and all the input pins of all the converters strictly on the filter's output side.

- *Ishare* pins. This connection allows the communication of current share information among the paralleled units. The voltage on each *Ishare* pin is internally referenced to its local *Vin(-)* pin, and determines that unit's output current relative to the other converters' currents. To ensure accurate sharing of load current information, all the *Vin(-)* pins should be tied together so they are at the same potential. The interposing of components between different *Vin(-)* pins will lead to undesirable voltage shifts and

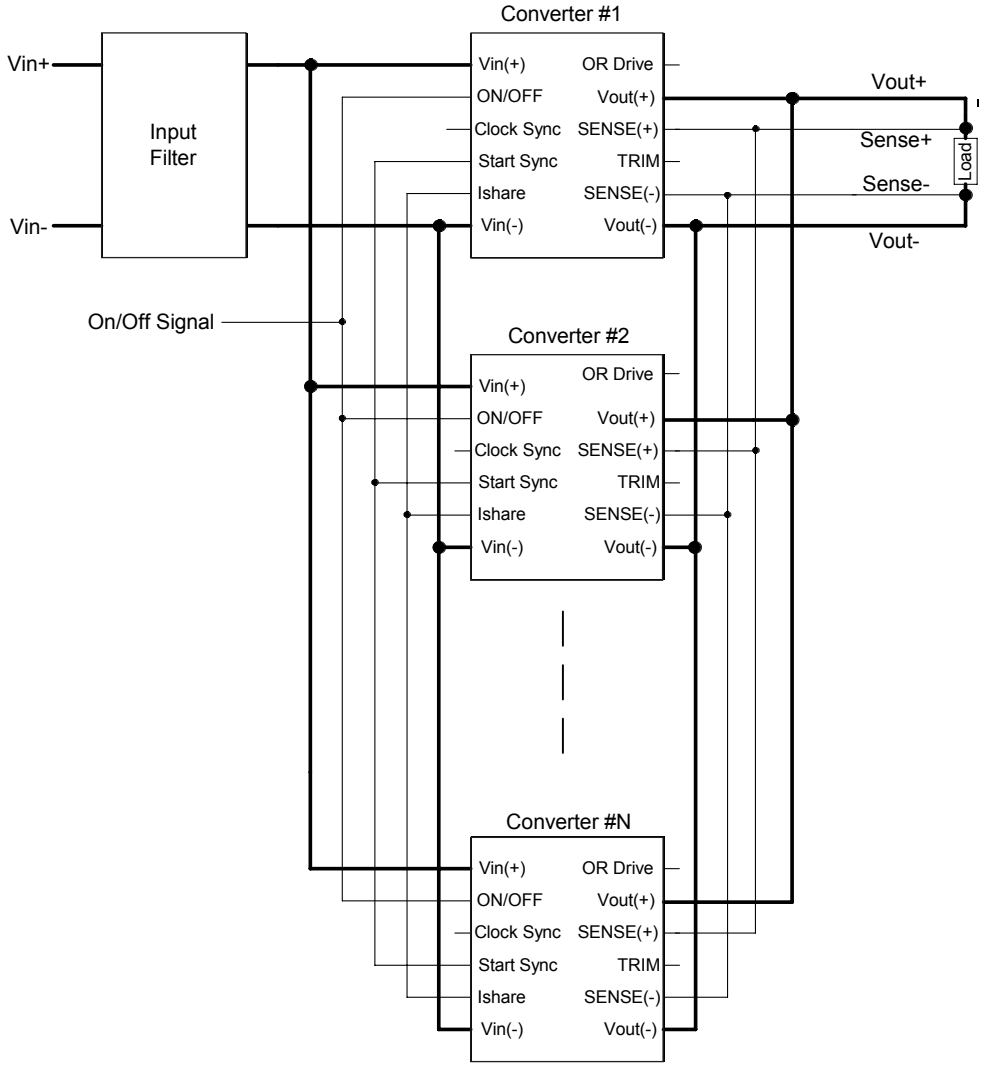

Figure 2: Basic Parallel Connection of *N PowerQor* Converters

noise that will increase the current sharing error among the units.

- Like remote sense pins *SENSE(+)* and *SENSE(-)*. The like remote sense pins of different units should all be tied together at the point at the load where it is desired to regulate the load voltage. The traces running from the load to the remote sense pins should be distinct from those carrying the load current. If this separation is not observed the load current will cause potential differences in the signals to the remote sense pins which will adversely effect the load voltage regulation.

- Like output voltage pins *Vout(+)* and *Vout(-)* if redundancy is not required. If redundancy is required the *Vout(-)* pins are separately connected to OR'ing elements. *(See OR'ing Function section)*

- Start synchronization pins *(Start Sync)*. This ensures that the converters turn on gracefully without false starts or output voltage glitches, especially when the load current exceeds the rated current of one module. (Start Synchronization section)

- *ON/OFF* pins, when converters with the same turn-on polarity must be powered up and down together by the same signal. A TTL-level on/off signal should be used. The connected *Start Sync* pins ensure that all the converters turn on together gracefully. The *ON/OFF* pins can be driven by separate signals when it is desired to turn individual converters on and off selectively. Even without any OR'ing circuitry, paralleled *Power*Qor converters are designed to operate correctly with some of them turned off, provided none of the idle converters are faulty.

The current-sharing arrangement described above is valid for any number of paralleled modules. Master-slave current sharing has no adverse effects on the load, voltage, or temperature regulation of the output voltage.

Also note that it is necessary to connect an electrolytic capacitor at the input of the paralleled *Power*Qor converters to prevent input instability. Refer to [1] for a complete discussion of this problem that includes the preferred remedy.

Start Synchronization

The Start Synchronization feature of *Power*Qor converters gives the user complete control over the relative start up and shut down times of individual converters in multi converter systems. The *Start Sync* pins of all groups of converters that must be turned on and off simultaneously are connected together. Start-up and shut down signals with the desired phases are then sent to the appropriate groups of converters to activate or deactivate them. Note that this feature is designed for use not just in paralleled systems, but in any arbitrary system utilizing *Power*Qor converters of any combination of output voltages or ratings.

The *Start Sync* feature is particularly useful in paralleled systems to avoid faults and output voltage glitches at turn on, as explained below.

*Power*Qor converters use a sophisticated scheme utilizing an on-board microprocessor to respond to fault conditions, including output over-current conditions. Upon first detecting an over-current fault the microprocessor shuts down the converter for 200ms. At the end of this period the converter attempts to restart. If the fault persists and the output voltage does not rise to a valid value in 20ms, the microprocessor shuts the converter down again for 200ms. This hiccup mode continues until the fault goes away and normal converter operation is restored.

When converters are paralleled, it is essential for them to turn on at exactly the same time in response to a com-

mand from the ON/OFF signal. Otherwise, in a system where the load current exceeds the capabilities of one converter, the first unit that comes up will immediately go into current limit. For a *Power*Qor converter this is the hiccup mode just described. While one converter is in its 200ms off state, another converter will attempt to start, and will also go into current limit, and so on. Eventually after numerous false starts the converters will synchronize their start-ups, and the system will come up. However the start up waveform of the output voltage will be marred by glitches corresponding to those instances when converters were attempting to start up individually.

This problem has been solved elegantly in the *Power*Qor converters with the aid of a start synchronization circuit. The *Start Sync* pins of paralleled converters are connected together. The *Start Sync* pin of each converter is internally connected to its local microprocessor and serves a dual input/output function. While the converters are off all the *Start Sync* pins are at a logical high value. When a signal is received by the converters to run, the microprocessor of the first converter to start up immediately pulls down the *Start Sync* node. All the converters are monitoring the *Start Sync* node, and when it goes low it commands them to abandon whatever they are doing and immediately join in starting up. Consequently all the converters always start up simultaneously and the output voltage glitches are virtually eliminated.

Clock Synchronization

Each *Power*Qor full feature converter is equipped with a clock frequency synchronization *(Clock Sync)* pin that can be connected to an external clock to force the module to run at the frequency of the external signal. In general, synchronizing the clocks of the converters in any system, not just a paralleled one, can decrease the system's EMI production. Multiple converters are synchronized by tying all the clock sync pins together and driving them from the same source, as shown in Figure 3 for two units.

The clock synchronization signal for *Power*Qor full feature converters should be a TTL logic level square wave voltage with a duty ratio between 25% and 75%. **The frequency of the synchronization signal must be higher than the intrinsic switching frequency of the converters. The converters will be damaged by attempts to synchronize them to a frequency lower than that of their internal clock.** Since the nominal switching frequencies of *Power*Qor full-feature modules vary for different output voltages, the user should refer to the appropriate data sheet to determine the correct range of synchronization frequencies.

Synchronizing *N* paralleled converters to one clock has the effect of forcing all the individual input ripple currents to have the same frequency and phase, increasing the total ripple current to, $N \bullet i_R$, where i_R is the ripple current of one unit. All *Power*Qor converters have an internal input filter, so the ripple current they draw from the input voltage source is low. Nevertheless an external input filter is still required in the paralleled system, as explained in [1].

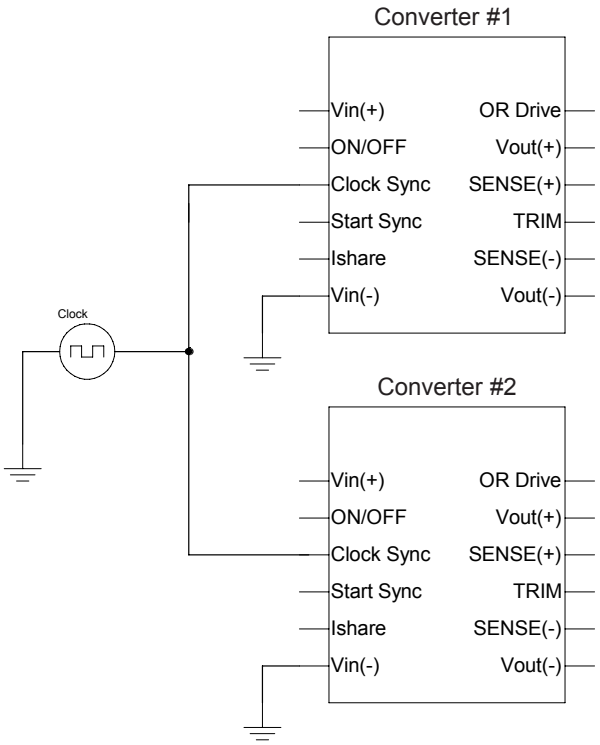

Figure 3: Simple Non-Interleaved Clock Synchronization

Furthermore, the total ripple current can be reduced even further by interleaving the clocks of the converters. The benefits of clock interleaving are especially pronounced in a paralleled system in which the various converter output currents are equal. In this case, not only can the ripple current be greatly reduced by interleaving, but it can be virtually eliminated under certain operating conditions. Another advantage is that the fundamental frequency of the ripple current increases from f_R to $f_R N$ where N is the number of clocks interleaved. Thus, compared to the non-interleaved case the external input filter in an interleaved system can be reduced substantially in size.

In general, if N units are paralleled they can be synchronized to a maximum of N differently phased clocks. The optimum phase of the j-th clock signal, in degrees, is $\theta_j = 360 \bullet (j - 1)/N$. For example, 3 clocks should be phased at intervals of 0, 120 and 240 degrees.

Using N clocks for N converters can be impractical, and the number of clocks can be reduced to M, with each clock driving N/M converters. The ripple current, though now greater than with N clocks, is still less than in the non-interleaved case.

For example, half the converters of an even total number N can be synchronized to one clock and the other half to a clock in anti-phase. The actual implementation of the interleaving for this case using *Power*Qor full feature converters is particularly simple. Because *Power*Qor converters can be synchronized with a square wave signal, the second clock can be derived by simply inverting the first one, as illustrated in Figure 4.

The foregoing discussion notwithstanding, it should be noted again that the ripple current of paralleled *Power*Qor converters is so low that in general, it is not necessary to interleave the modules.

Although *Power*Qor converters will synchronize to much higher frequencies than those suggested in the datasheets, the user is advised against violating the limit, for two reasons. First, higher frequency operation is less efficient due to increased switching losses. Second, above a certain higher frequency, the maximum duty ratio that the converters are capable of producing begins to decrease. The converters can then run out of duty ratio at low line, leading to loss of regulation and a reduced output voltage.

When it is not used the *Clock Sync* pin should be left open.

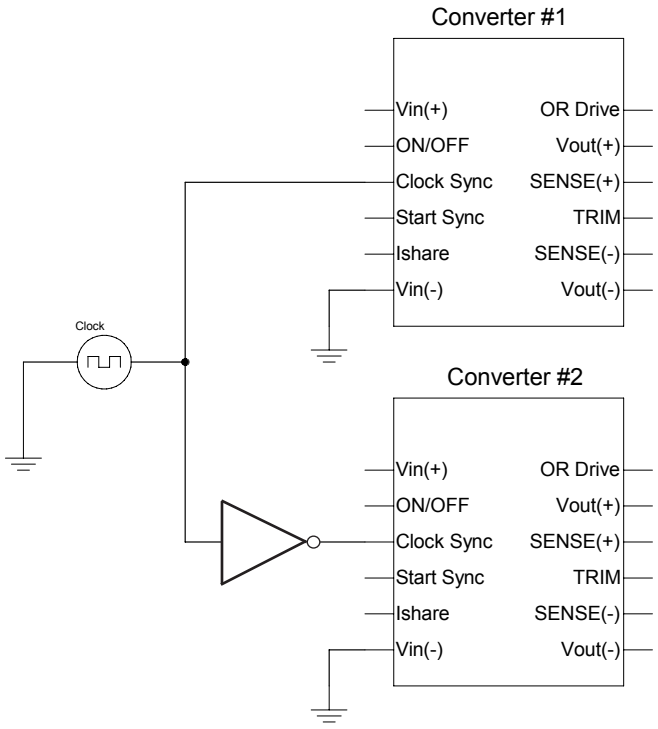

Figure 4: Interleaved Clock Synchronization

No-Load Operation

A characteristic feature of the no-load behavior of paralleled *Power*Qor converters should be noted. A *Power*Qor converter will sink a "back-drive" current of typically up to 5% of the full load current if its output is connected to a voltage source higher than its output voltage. Similarly, in a paralleled system with no external load, the higher voltage units will back drive the lower voltage units. Therefore, at no load, some of the converters will become sources and others sinks, and small positive and negative output currents will accordingly be seen among the converters, with the total current adding to zero. Note that other synchronous rectifier converters available on the market offer no back-drive protection and permit the unwanted effect of allowing the sink converters to be back driven by the maximum output current that the source converters can supply.

Output Voltage Trim

A stand-alone *Power*Qor converter is trimmed up with a resistor connected between the trim pin *(TRIM)* and the positive remote sense pin *(SENSE(+))*. It is trimmed down with a resistor connected between *TRIM* and *SENSE(-)*. Refer to the appropriate data sheet for the component values. In order for the regulation of the output voltage to remain as tight as in the untrimmed case, the traces from the trim resistors to the sense pins must be routed separately from any traces carrying load current.

The output voltages of paralleled *Power*Qor full feature converters can be separately trimmed up or down in exactly the same way that a stand-alone converter would be. Refer to the data sheet for the trimming procedure. Note that converters should all be trimmed to the same output voltage. The current sharing accuracy and output voltage regulation are unaffected by trimming. Use 1% trimming resistors to ensure that trimming does not add extra tolerance to the output voltage set-point, which could cause it to fall outside the range of adjustment of the current share circuit or make it hit the over-voltage trip point.

Mixing of Kilo, Mega, Giga and Tera Converters

A particularly attractive feature of Kilo, Mega, Giga and Tera full feature converters is that they are all freely mixable in paralleled systems, if they are of the same output voltage. The units will then share the load current in proportion to their ratings.

As an example, the rated output currents of 48Vin to 2.0Vout Kilo, Mega, Giga and Tera converters are respectively 20, 30, 40 and 60 amps. If a paralleled system utilizing one of each of these units has a total load current of 120 A, the Kilo, Mega, Giga and Tera units will supply 16, 24, 32 and 48 A, respectively, of the total output current. Thus each converter will supply 80% of its rated current. The thermal, voltage and current stresses will therefore be evenly distributed among the converters.

As another example, if two Kilos and one Mega are paralleled at a total load current of 50A each Kilo will supply 15A and the Mega will supply 20A. Again the ratio of the output current to the rated current is the same for all the converters. This relationship holds for any arbitrary combination of Kilo, Mega, Giga and Tera modules.

Mixing the converters does not effect the clock synchronization function because all members of the same output voltage family switch at the same frequency. The clock sync pins are connected together just as before, as are the start sync pins, and of course, the *Ishare* pins. The output voltages of the converters, which must be set at the same nominal value, can be trimmed in the usual way.

OR'ing Function

*Power*Qor full-feature converters can be used in redundant systems by connecting them to the common output bus through an OR'ing circuit. Because the *Power*Qor converters produce high output currents at low output voltages, diodes should not be used as the OR'ing elements, since they have relatively large forward voltage drops. For example, an OR'ing diode with a forward voltage drop of 0.3V used at 60A with a 48Vin to 1.5Vout converter would dissipate 18W, or 20% of the output power. This is a very severe penalty to pay for this function.

A better solution is to use low resistance MOSFETs with low drain-source resistance as the OR-FETs, or OR'ing elements. MOSFETs with resistances of just a few milliohms that can be used for this purpose are readily available in the commercial market. The disadvantage of OR-FETs is that they need to be gated on and off at the proper times by a control circuit. The control circuit and the OR-FETs need a source of power.

To address this need every *Power*Qor full feature converter is equipped with an *OR-Drive* pin which supplies a voltage higher than the output voltage that can be used to enhance an OR-FET. Designers of OR-FET drive circuits that utilize the voltage at the *OR-Drive* pin should be aware that the current that this pin can provide is very limited because it is connected to the internal voltage source through a fairly high value resistor of not less than 2.26 kΩ. Refer to the appropriate datasheet for the series resistor value and the open-circuit *OR-Drive* pin voltages.

Full Feature Evaluation Board

SynQor has developed a test board for the evaluation of two paralleled *Power*Qor converters, which is available for sale from SynQor directly or through our website [5]. The evaluation board contains the following:

- A clock external to the converters which can be set by the customer to the correct synchronization frequency for the output voltage being tested. The clock can be configured to drive the converters in phase, or in anti-phase for interleaved operation.
- BNC connectors for input voltage and output voltage monitoring. The output voltage connector allows accurate measurements to be made of output voltage regulation and noise.
- BNC connectors for the accurate measurement of the average output currents of the individual converters to allow for evaluation of the current-sharing accuracy.
- Current loops in the input current and the individual output current paths allowing for detailed oscilloscope examination of the respective currents.
- A master as well as local ON/OFF switches.

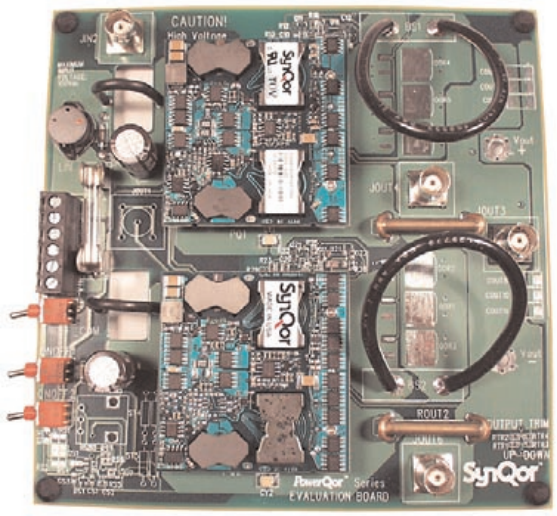

Figure 5: Full-feature Evaluation Board

Output currents are measured with voltmeters connected to the BNC connectors via the voltage developed across 1 mΩ shunts. The shunts have different grounds, so care must be taken to float the voltmeters.

Impedance Matching in the Layout

The current share circuitry in each converter is referenced to its primary ground, *Vin(-)*. All the *Vin(-)* pins of the converters are connected to a common node which, through an input filter, connects to the negative terminal of

the input voltage source. If the impedance from the *Vin(-)* pin to the common node is different from converter to converter, input current flow will cause the potential drop across the various impedances to be different, and the potentials of the *Vin(-)* pins will shift relative to each other. Since all the *Isense* pins are connected together, the relative internal voltages in the current share circuits will also shift. This will introduce additional current sharing error among the converters.

To mitigate this problem, the impedance differences should be minimized by laying out the converters on the motherboard as symmetrically as possible with respect to the current paths from the common negative node to the converters. As stated before, all the *Vin(-)* pins must be connected directly together on the output side of the filter.

Impedance matching on the output side is just as important. If the impedances between the output pins of the individual modules and the remote sensing point are mismatched, the output voltages of the converters will be different. Thus, when the output voltage is trimmed up, the voltage of the converter with the highest impedance path to the load may rise high enough to cause an over-voltage fault. Also, the added error among the individual output voltages of the converters could cause the total voltage deviation to exceed the limits of adjustment of the current share circuit. Again, the problem should be minimized by laying out the current-carrying traces from the converters to the load as symmetrically as possible.

References

1. "Input System Instability", SynQor Application Note PQ-00-05-1 Rev. 01, available by request from SynQor or on our website at www.synqor.com.

2. V. J. Thottuvelil and G. C.Varghese, "Stability analysis of paralleled dc/dc converters with active current sharing," in IEEE Power Electronics Specialists Conference, 1996, pp. 10870-1086.

3. V. J. Thottuvelil and G. C. Varghese, "Analysis and control design of paralleled dc/dc converters with current sharing," in IEEE Transactions on Power Electronics, Vol. 13, No. 4, July 1998.

4. Full-Feature evaluation boards available for sale from SynQor by calling (508) 485-8434 or purchase over our website at www.synqor.com.

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